

Express Mail Label EV336676431US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: JACK ZEZHONG PENG

APPLICATION NO.: TO BE ASSIGNED

FILED: HEREWITH

FOR: HIGH DENSITY SEMICONDUCTOR MEMORY CELL
AND MEMORY ARRAY USING A SINGLE
TRANSISTOR AND HAVING COUNTER-DOPED
POLY AND BURIED DIFFUSION WORDLINE

EXAMINER:

ART UNIT:

CONF. NO:

**Information Disclosure Statement Within Three Months of
Application Filing or Before First Action – 37 C.F.R. § 1.97(b)**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

1. Timing of Submission

This information disclosure is being filed within three months of the filing date of this application or date of entry into the national stage of an international application or before the mailing date of a first Office action on the merits, whichever occurs last [37 C.F.R. § 1.97(b)]. The references listed on the enclosed Form PTO-1449 (modified) may be material to the examination of this application; the Examiner is requested to make them of record in the application.

2. Cited Information

☒ Copies of the following references are enclosed:

- ☐ All cited references
- ☐ References marked by asterisks
- ☒ The following: All Non-US Patent References

☐ Copies of the following references can be found in parent U.S. Application No. :

- ☐ All cited references
- ☐ References marked by asterisks
- ☐ The following:

- ☒ This application was filed after 30 June 2003 and no copies of U.S. patents nor published applications are enclosed (See Notice of Deputy Commissioner Kunin on 11 July 2003).
- ☒ The following references are not in English. For each such reference, the undersigned has enclosed (i) a translation of the reference; (ii) a copy of a communication from a foreign patent office or International Searching Authority citing the reference, (iii) a copy of a reference which appears to be an English-language counterpart, or (iv) an English-language abstract for the reference prepared by a third party. Applicant has not verified that the translation, English-language counterpart or third-party abstract is an accurate representation of the teachings of the non-English reference, though, and reserves the right to demonstrate otherwise.
 - ☐ All cited references
 - ☐ References marked by ampersands
 - ☒ The following: JP61292295

3. Effect of Information Disclosure Statement (37 C.F.R. § 1.97(h))

This Information Disclosure Statement is not to be construed as a representation that: (i) a search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the cited information is, or is considered to be, material to patentability. In addition, applicant does not admit that any enclosed item of information constitutes prior art to the subject invention and specifically reserves the right to demonstrate that any such reference is not prior art.

4. Fee Payment

No fees are believed due because this Information Disclosure Statement is being filed before the mailing date of the first Office Action.

- ☐ Applicant further submits that no fee is due in light of the following certification under 37 C.F.R. § 1.97(e) (check only one):
 - ☐ In accordance with 37 C.F.R. § 1.97(e)(1), the undersigned hereby states that each item of information submitted herewith was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement; or
 - ☐ In accordance with 37 C.F.R. § 1.97(e)(2), the undersigned hereby states that no item of information submitted herewith was cited in a communication from a foreign patent office in a counterpart foreign application, or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any

individual designated in 37 C.F.R. § 1.56(c), more than three months prior to the filing of this statement.

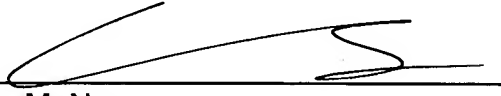
However, should the Commissioner determine that fees are due in order for this Information Disclosure Statement to be considered, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 50-0665.

5. Patent Term Adjustment (37 C.F.R. § 1.704(d))

- ☐ The undersigned states that each item of information submitted herewith was cited in a communication from a foreign patent office in a counterpart application and that this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this statement. 37 C.F.R. § 1.704(d).

Respectfully submitted,
Perkins Coie LLP

Date: 3/10/04


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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Form PTO-1449 (Modified) (Use several sheets if necessary)				COMPLETE IF KNOWN	
				Application Number	
				Confirmation Number	
				Filing Date	
				First Named Inventor	Jack Zezhong Peng
				Group Art Unit	
				Examiner Name	
Sheet	1	of	4	Attorney Docket No.	384848014US

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.	U.S. Patent or Application		Name of Patentee or Inventor of Cited Document	Date of Publication or Filing Date of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		NUMBER	Kind Code (if known)			
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		4,322,822		McPherson	03/30/82	
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EXAMINER	DATE CONSIDERED
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		NUMBER	Kind Code (if known)			
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		NUMBER	Kind Code (if known)			
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Examiner Initials*	Cite No.	Foreign Patent or Application			Name of Patentee or Applicant of Cited Document	Date of Publication or Filing Date of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
		Office	NUMBER	Kind Code (if known)				
		EP	0 295 935	A1	Advanced Micro Devices, Inc.	12/21/88		
		JP	61292295		Fujitsu Ltd.	12/23/86		

OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume issue number(s), publisher, city and/or country where published.	T
		MIRANDA, ENRIQUE et al; Analytic Modeling of Leakage Current Through Multiple Breakdown Paths in SiO2 Films; 39 th Annual International Reliability Physics Symposium; Orlando, FL 2001.	
		LOMBARDO, S. et al; Softening of Breakdown in Ultra-Thin Gate Oxide nMOSFET's at Low Inversion Layer Density; 39 th Annual International Reliability Physics Symposium; Orlando, FL 2001.	
		WU, E.W. et al; Voltage-Dependent Voltage-Acceleration of Oxide Breakdown for Ultra-Thin Oxides; IEEE, 2000.	
		RASRAS, MAHMOUD et al; Substrate Hole Current Origin After Oxide Breakdown; IEEE, 2000.	

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		SUNE, JORDI et al; Post Soft Breakdown Conduction in SiO ₂ Gate Oxides; IEEE, 2000.	
		DeGRAAF, C., et al, A Novel High-Density Low-Cost Diode Programmable Read Only Memory, IEEE, 1996.	

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